CLAIMS

What is claimed is:

1. A manufacturing process for forming a barrier layer comprising:

providing a polysilicon plug having a surface in a portion of a dielectric layer of a portion of an integrated circuit;

depositing a layer of titanium on at least a portion of the surface of the polysilicon plug;

depositing a layer of amorphous material on at least a portion of the layer of titanium; and

depositing a layer of titanium nitride on at least a portion of the layer of amorphous material.

2. The method of claim 1, further comprising:

forming a recess in a portion of the polysilicon plug; and

forming a well including a portion of the dielectric layer above the polysilicon plug;

depositing portions of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride within the well and over at least a portion of a surface of the dielectric layer; and

removing at least a portion of each of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the at least a portion of the surface of the dielectric layer.

3. The method of claim 1, further comprising:

placing the dielectric layer of an integrated circuit in a low-pressure chemical vapor deposition chamber;

providing a carrier atmosphere in the low-pressure chemical vapor deposition chamber having a pressure in a range between about 0.1 Torr to about 100 Torr;

providing a precursor compound in the low-pressure chemical vapor deposition chamber; and

heating the dielectric layer to a temperature in a range of between about 200°C to about 600°C.

4. The method of claim 3, wherein the carrier atmosphere comprises a mixture including at least one gas selected from a group consisting of a noble gas, nitrogen and hydrogen.

5. The method of claim 3, wherein the precursor compound comprises an organo-metallic compound.

6. The method of claim 5, wherein the precursor compound comprises tetrakis-dialkylamido-titanium.

7. The method of claim 2, wherein the removing the at least a portion of each of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the surface of the dielectric layer comprises planarizing the dielectric layer to remove at least the portions of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the at least a portion of the surface of the dielectric layer.

8. The method of claim 1, wherein the depositing the layer of amorphous material comprises depositing a layer of titanium carbonitride having an amorphous structure substantially without grain boundaries therein.

9. The method of claim 1, wherein the depositing the layer of amorphous material comprises depositing a layer of substantially amorphous material substantially without crystal grain boundaries therein.

10. The method of claim 8, wherein the depositing the layer of titanium carbonitride comprises depositing a layer of titanium carbonitride having a ratio of carbon to nitrogen therein in the range of from about 1:5 to about 1:20.

11. The method of claim 6, wherein the precursor compound comprises a sole precursor.

12. A method for forming a barrier layer comprising:

providing a polysilicon plug having a surface in a portion of a dielectric layer of a circuit;

depositing a layer of titanium on at least a portion of the surface of the polysilicon plug;

depositing a layer of amorphous material on at least a portion of the layer of titanium; and

depositing a layer of titanium nitride on at least a portion of the layer of amorphous material.

13. The method of claim 12, further comprising:

forming a recess in a portion of the polysilicon plug; and

forming a well including a portion of the dielectric layer above and the recess in the polysilicon plug;

depositing portions of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride within the well and over at least a portion of a surface of the dielectric layer; and

removing at least a portion of each of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the at least a portion of the surface of the dielectric layer.

14. The method of claim 12, further comprising:

placing the dielectric layer of an integrated circuit in a low-pressure chemical vapor deposition chamber;

providing a carrier atmosphere in the low-pressure chemical vapor deposition chamber having a pressure in a range between about 0.1 Torr to about 100 Torr;

providing a precursor compound in the low-pressure chemical vapor deposition chamber; and

heating the dielectric layer to a temperature in a range of between about 200°C to about 600°C.

15. The method of claim 14, wherein the carrier atmosphere comprises a mixture including at least one gas selected from a group consisting of a noble gas, nitrogen and hydrogen.

16. The method of claim 14, wherein the precursor compound comprises an organo-metallic compound.

17. The method of claim 16, wherein the precursor compound comprises tetrakis-dialkylamido-titanium.

18. The method of claim 13, wherein the removing the at least a portion of each of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the surface of the dielectric layer includes planarizing the dielectric layer to remove at least the portions of the layer of titanium, the layer of amorphous material, and the layer of titanium nitride deposited on the at least a portion of the surface of the dielectric layer.

19. The method of claim 12, wherein the depositing the layer of amorphous material comprises depositing a layer of titanium carbonitride having an amorphous structure substantially without grain boundaries therein.

20. The method of claim 12, wherein the depositing the layer of amorphous material comprises depositing a layer of substantially amorphous material having few crystal grain boundaries therein.

21. The method of claim 19, wherein the depositing the layer of titanium carbonitride comprises depositing a layer of titanium carbonitride having a ratio of carbon to nitrogen therein in the range of from about 1:5 to about 1:20.

22. The process of claim 14, wherein the precursor compound comprises a sole precursor.